**Quartz Tuning Fork Sensor**

**Project Documentation**

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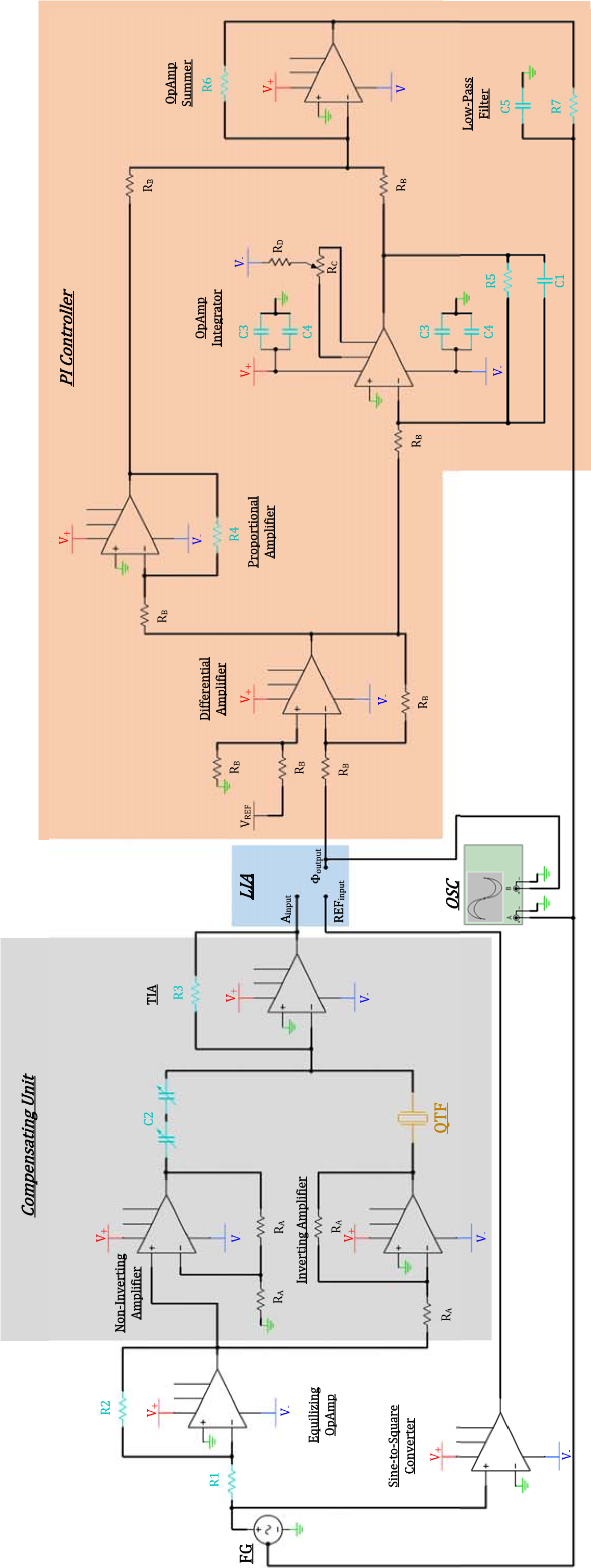
# Overview

## General

Refer to Fig. 1 for a complete circuit diagram.

Used Abbreviations:

* DPP – Dual Power Supply
* FG – Function Generator;
* OSC – Oscilloscope;
* LIA – Lock-In Amplifier;
* QTF – Quartz Tuning Fork;
* OpAmp – Operational Amplifier;
* TIA – Transimpedance Amplifier;
* – Instrument component of the project;
* – Green connector in project circuit;
* – Black connector in project circuit;
* – Indicating light parameter on LIA;

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**Fig. 1.** Circuit diagram of a basic QTF Sensor

## Function Generator (FG)

FG allows to supply circuits with AC current inputs. Besides the common application of supplying sinusoidal AC signal source, the project implies the use as DC signal source and modulation of sinusoidal AC signal

* DC Signal: the problem with DC power supplies arises when one wants to determine reading for voltage in opposite direction of what been tested currently (involves cumbersome process of switching connections). However, FG allows to circumvent the problem, as signal offset can be easily changed around 0V. To approximate DC, FG can be set into noise waveform with minimal possible amplitude. At this point, changing the offset of the noise waveform is equivalent to changing DC voltage.
* Frequency Modulation: since ambient conditions change resonant frequency of the QTF, it is necessary to have the circuit adjust the operating frequency to the new resonance in real time. Modulation of the signal allows to shift operating frequency around the center value based on input DC voltage. The relationship is linear and is described by Eq. 1

## Sine-to-Square Converter

Due to FG’s inability to provide reference signal that can be modulated, a unit was designed to provide a square wave reference signal for LIA. The unit utilizes the concept of voltage saturation by OpAmp to the level of DC voltage OpAmp is powered with. As soon as input signal of the unit, like sine wave, passes a small threshold, it is saturated; when input signal changes sign, the saturation occurs to the other limit. Thus, output signal is approximated as a square wave.

It is important to note that 2 parameters impact the mentioned approximation: amplitude of the input signal and OpAmp powering voltages. If the amplitude of the input signal is insufficient, the saturation of the signal will not be nearly-instantaneous, but have some curvature from the input sine wave. As for as OpAmp powering voltages, ensuring that they are equal guarantees that wave spend saturated equally in both “directions”.

## Voltage Dropper

The unit pursues 2 goals:

* Equalize input impedance between sine-to-square converter and the compensating unit. This is achieved by having the unit being based on OpAmp, similarly to sine-to-square converter
* To reduce the voltage amplitude used for setting QTF in resonance since excess voltage may damage QTF. This is accomplished on the basis of inverse amplifier; if Connector R1 resistor is larger than Connector R2 resistor, the gain can be described by Eq. 2.

## Compensating Unit

The unit pursues 2 purposes:

* Supply QTF with a voltage signal to excite prong oscillation and consequently convert the QTF output current to voltage for further analysis. This is accomplished with the use of TIA. IA performs current-voltage conversion per Eq.3, and with the output signal depending on resistor in Connector R3.
* Perform parasitic capacitance compensation. To achieve that, QTF and to compensating capacitor in Connector C2 need to be supplied with opposite voltages; in such case signal from compensating capacitor will eliminate parasitic capacitance, leaving only QTF signal.

QTF branch of the unit is supplied through inverting amplifier. However, resistors were chosen to be the same, making it so that the gain of the amplifier is -1.

Connector C2 branch is supplied through non-inverting amplifier. By choosing equal resistors for the amplifier, the gain results to be 2. Such gain signifies that compensating capacitor will need to be only half of the parasitic capacitance value.

## Lock-In Amplifier

LIA provides a unique opportunity to analyze QTF output signal. It performs the following main objectives:

* Performs filtering of the QTF output to the frequency of the reference with high efficiency. This allows not to be concerned with RC filtering.
* Allows to measure the strength of the QTF output signal. This allows to observe resonant peak of the QTF. In addition, it provides numeric values necessary to perform capacitance compensation; by checking frequencies left and right of the peak, it allows to gauge on the quality of compensation.
* Provides the value for phase difference between the QTF output and the reference signal, which is necessary to frequency adjustment in phase-locked loop.

## Proportional Gain Unit

The unit pursues is part of the controller necessary for phase-locked loop. If the circuit sense deviation from a set point, proportional gain unit brings the difference down. The basis for the unit is inverting amplifier with the gain dependant on resistor in Connector R4 by Eq. 4.

However, proportional gain has intrinsic steady-state error: once desired value is reached, the unit action is stopped. This causes difference to increase, causing consequent reactivation of the unit. Thus, the steady-state error oscillates around the set point value.

## Integral Gain Unit

In order to resolve the issue of steady-state error, integral gain unit is placed in parallel with the proportional gain. The unit utilizes capacitor in Connector C1 to bring the steady state error to zero. To prevent drifting, a resistor in Connector R5 has also been introduced.

## Summing Amplifier

The unit brings proportional and integral outputs together by summing the respective voltages. As part of the unit, resistor in Connector R6 may be changed to control the gain (Eq.5), though it is recommended to keep the gain equal to -1.

# Module Verification

Prior to verifying the modules, ensure that the circuit is powered (refer to 3.1)

## Sine-to-Square Converter

1. Connect AC sinusoidal signal to Port 2;
2. Connect OSC to Port 3;
3. You are expected to see a square wave signal on OSC (which means conversion is performed correctly);

## Voltage Dropper

1. Take measurement of 2 resistors such that they have a factor difference;
2. Place larger resistor in Connector R1, and smaller resistor in Connector R2;
3. Connect AC sinusoidal signal to Port 4;
4. Connect OSC to Port 5;
5. You are expected to see the amplitude of the signal on OSC to be a fraction of what being supplied (per Eq. 2);

## Compensating Unit

1. Connect AC sinusoidal signal to Port 6. Set amplitude of AC signal to no approximately 500mV;
2. Connect OSC to Port 7;
3. Place QTF in Connector QTF;
4. Set AC signal to 32.7kHz and begin to increase frequency by 1Hz at a time;
5. You are expected to observe the rapid increase in signal strength until ~32.75kHz, followed by rapid decrease;

## Differential Amplifier

1. Connect 1st DC voltage source to Port 10;
2. Connect 2nd DC voltage Source to Port 11;
3. Connect measuring device (voltmeter/OSC) to Port 12;
4. You are expected to measure voltage according to Eq. 6;

## Proportional Gain Unit

1. Take measurement of a resistor such that they have a factor difference;
2. Place the resistor in Connector R4;
3. Connect AC sinusoidal signal to Port 13;
4. Connect OSC to Port 5;
5. You are expected to see the amplitude of the signal on OSC to be a fraction of what being supplied (per Eq. 4);

## Integral Gain Unit

1. Connect AC square-wave signal to Port 15;
2. Connect OSC to Port 16;
3. You are expected to observe the output signal to be triangular wave; it may require to adjust frequency to observe the effect, depending on the values of capacitor in Connector C1 and resistor in Connector R5.

## Summing Amplifier

1. 1. Connect 1st DC voltage source to Port 17;
2. Connect 2nd DC voltage Source to Port 18;
3. Connect measuring device (voltmeter/OSC) to Port 19;
4. You are expected to see the measured voltage to according to Eq. 7;

# Instrument Setup

## Dual Power Supply (DPP)

Fig. 2 presents diagram of setting up DPP necessary for powering the sensor. Recommended supply voltage is around 10V.

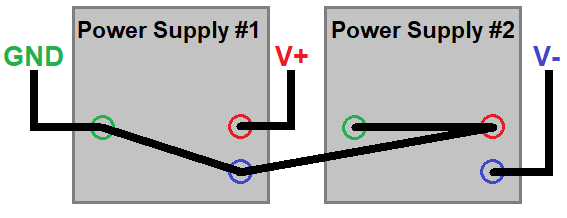


Fig. 2

## Port Connections

Following port connections are required for the operation of the sensor circuit. It is recommended that you connect modules in steps, ensuring that they all work correctly.

1. Port + with positive voltage from DPP;
2. Port – with negative voltage from DPP;
3. Port GND with ground from DPP;
4. Port 1 with FG that will be powering QTF (main FG);
5. From Port 1, run wire connection to Port 2 and Port 4;
6. Port 3 with REF input of LIA;
7. From Port 5, run wire to Port 6;
8. Port 7 with A input of LIA;
9. Port 10 with reference FG;
10. Channel 2 output of LIA with Port 11 and OSC;
11. From Port 12, run wire to Port 13 and Port 15;
12. From Port 14, run wire to Port 17;
13. From Port 16, run wire to Port 18;
14. Port 19 with modulation input of main FG connected to Port 1;

## Sine-to-Square

1. Turn on AC sinusoidal signal on main FG;
2. Confirm that output of Port 3 is a square wave;
3. Increase the amplitude of AC sinusoidal signal on main FG so that square wave output of Port 3 is sharpest (around 5Vpp);
4. Adjust voltage on DPP so that square wave is symmetrical around 0V;

## Voltage Dropper

1. Turn on AC sinusoidal signal on main FG;
2. Confirm that output of Port 5 is a sinusoidal wave with smaller amplitude than the input signal;
3. Adjust the choice of resistors in Connector R1 and Connector R2 so that the output signal at Port 5 is around 500mV;

## Compensating Unit

1. Ensure that steps 1-8 of Section 3.2 are completed;
2. Turn on AC sinusoidal signal on main FG. You are expected to observe light UNLK on LIA to turn off;
3. Set LIA to following parameters:
   1. Signal Filters: all OUT;
   2. Signal Inputs: A;
   3. Sensitivity: 500 mV;
   4. Dyn Res: Low;
   5. Channel 1:
      1. Offset: Off;
      2. Expand: x1;
   6. Channel 2:
      1. Offset: Off;
      2. Expand: x1;
   7. Display: R – Φ;
   8. Reference:
      1. Mode: f;
      2. Trig: sine wave;
   9. Time Constant:
      1. Pre: 100 ms;
      2. Post: 0.1 s;
4. Set AC signal on main FG to 32.7kHz and begin to increase frequency by 1Hz at a time; You are expected to observe the rapid increase in signal strength until ~32.75kHz, followed by rapid decrease;
5. Determine the frequency, at which left scale reaches maximum value (resonant frequency f0);
6. Adjust resistor in Connector R3 small steps so that left scale reading at f0 is around 350mV. If at any point during the calibration light OVLD blinks, it means the signal from compensating unit is too large and Connector R3 resistor needs to be reduced;
7. Connecter compensating capacitor assembly to Connector C2;
8. Begin adjusting compensating capacitor in following manner;
   1. Set main FG to f0, observe left scale value;
   2. Change frequency on main FG to f0+1Hz and f0-1Hz, observe left scale value;
   3. If observed values differ by more than 0.5, adjust compensating capacitance;
   4. Perform steps a-c until equal results around f0;
9. Set main FG to f0, and adjust offset of the right scale so it reads 0;
10. Obtain data verifying resonant peak. Recommended method:
    1. Perform frequency sweep at 0.1-0.2Hz per step, for a total of ±1-2Hz around f0;
    2. While sweeping, record both left and right scale readings;
    3. Perform 3 forward and 3 backward sweeps: f0🡪 +end 🡪 -end 🡪 +end 🡪 -end 🡪 +end 🡪 -end 🡪 f0 (results in most of frequency points being measured 6 times);
    4. Plot the obtained data; observe hysteresis and time evolution of the measurements;
    5. Perform Grubbs test analysis to on the obtained data, rejecting outliers
    6. Obtained the averaged measurement plots of your data;
    7. Evaluate plots from steps d and f and make judgement on quality of parasitic capacitance compensation;

## Frequency Modulation

1. Ensure that steps 1-14 of Section 3.2 are completed;
2. Set main FG sinusoidal signal to f0;
3. Adjust LIA’s right scale offset so that it reads 0;
4. Set timescale of LIA to 10s;
5. On main FG, activate modulation:
   1. Type: Frequency Modulation (FM);
   2. Source: External;
   3. Deviation: depends on the plots obtained as part of Section 3.5; recommended 2.5Hz;
   4. You are expected to observe flatline of LIA Channel 2 output on OSC;
6. One step at a time, decrease the time scale; if the flatline begins to oscillate, it means the timescale is too short;
7. Set reference FG to noise waveform of minimal possible amplitude; turn on the output;
8. Adjust the potentiometer so LIA Channel 2 output reads 0V;
9. Change the offset of the reference FG; You are expected to observe LIA Channel 2 output to match the chosen offset;
10. Continue to adjust reference FG offset in small steps to determine:
    1. Difference between specified offset and LIA Channel 2 output flatline;
    2. At what specified offset LIA Channel 2 no longer follows;
11. Following is the order of operation for determining the effect of resistors and capacitor in PI Control Unit:
    1. Turn off modulation of main FG;
    2. Switch the component of interest (Connector R4, Connector R5, Connector C1);
    3. Determine f0;
    4. Zero phase difference scale;
    5. Turn on modulation of main FG;
    6. Observe at what timescale LIA Channel 2 output stops being flatline;
    7. Observe how LIA Channel 2 output follows reference voltage;
    8. Ideally, one wants to minimize timescale, while also obtaining the best following.